In the Claims

Applicants have submitted a new complete claim set showing marked up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Please amend pending claims 6 and 7 as noted below.

Please add new claims 8-30 as noted below.

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1. (Original) A method for regenerating a clock signal based on a flip-flop and on two complementary signals at the clock rate, the flip-flop being connected as a divider by two of a combination of shaping signals each translating a direction, respectively rising or falling, of the edges of one of the complementary signals, wherein one of said shaping signals is used to reset the flip-flop.

2. (Original) The method of claim 1, applied to regenerating a clock signal downstream of a capacitive isolation barrier carrying the two complementary signals.

3. (Original) The method of claim 2, wherein an output of the flip-flop provides an image of a first one of said complementary signals, the flip-flop being reset on edges of the shaping signal of the other complementary signal.

4. (Original) A circuit for regenerating a clock signal based on two complementary signals by means of a D flip-flop, a clock input of which receives the result of a logic combination of two shaping signals resulting from a filtering of the respective rising edges of the complementary signals, wherein a reset input of the flip-flop receives one of said shaping signals.

5. (Original) The circuit of claim 4, wherein the logic combination is of NAND type, the shaping signals being provided by inverters.

6. (Currently amended) The circuit of claim 5, wherein the reset input of the flip-

flop is connected at the output of one of the inverters ~~inverter~~ for shaping the complementary signal, of which an output of the flip-flop provides an inverted image.

7. (Currently amended) An interface system between a modem and a transmission line, of the type using a capacitive isolation barrier to transmit a clock for modulating the signals to be transmitted from the modem to a processing circuit on the transmission line side of the interface system, including the clock regeneration circuit of claim 4.

8. (New) A clock signal regeneration circuit, comprising:

a first input for a clock signal and a second input for an inverted clock signal;

logic to shape the clock signal into a first signal and the inverted clock signal into a second signal;

a flip-flop; and

means for setting an initial state of the flip-flop after each alternate edge of the second signal.

9. (New) The clock signal regeneration circuit of claim 8, wherein the clock signal regeneration circuit is located on a line side of a capacitive isolation barrier.

10. (New) The clock signal regeneration circuit of claim 8, wherein the means for setting an initial state of the flip-flop comprises means for setting the initial state of the flip-flop after each rising edge of the second signal.

11. (New) The clock signal regeneration circuit of claim 8, wherein the flip-flop comprises a reset input, and wherein one of the first signal and the second signal is coupled to the reset input.

12. (New) The clock signal regeneration circuit of claim 8, wherein the logic comprises means for detecting each alternate edge of the clock signal and shaping the clock signal into a first signal having a single voltage pulse between each alternate edge of the clock

signal, and means for detecting each alternate edge of the inverted clock signal and shaping the inverted clock signal into a second signal having a single voltage pulse between each alternate edge of the inverted clock signal.

13. (New) The clock signal regeneration circuit of claim 12, wherein the logic comprises means for detecting each rising edge of the clock signal and shaping the clock signal into a first signal having a single voltage pulse between each rising edge of the clock signal, and means for detecting each rising edge of the inverted clock signal and shaping the inverted clock signal into a second signal having a single voltage pulse between each rising edge of the inverted clock signal.

AV 14. (New) The clock signal regeneration circuit of claim 8, wherein the logic comprises:

first and second resistors connected between the clock signal and the inverted clock signal;

a first capacitor coupled to the first clock signal and the first resistor; and

a second capacitor coupled to the inverted clock signal and the second resistor.

15. (New) The clock signal regeneration circuit of claim 14, wherein a reference voltage is coupled between the first and second resistors.

16. (New) The clock signal regeneration circuit of claim 14, further comprising a first inverter coupled to the first capacitor and a second inverter coupled to the second capacitor.

17. (New) The clock signal regeneration circuit of claim 16, wherein the output of the first inverter is the first signal and the output of the second inverter is the second signal.

18. (New) The clock signal regeneration circuit of claim 8, further comprising a NAND gate, wherein the first signal and the second signal are input to the NAND gate.

19. (New) The clock signal regeneration circuit of claim 18, wherein the flip-flop is a D-type flip-flop, and wherein an output of the NAND gate is input to a clock input of the flip-flop.

20. (New) The clock signal regeneration circuit of claim 19, wherein the flip-flop comprises a reset input, and wherein the second signal is coupled to the reset input.

21. (New) A method of regenerating a clock signal, comprising acts of:

shaping a clock signal into a first signal and an inverted clock signal into a second signal; and

setting an initial state of a flip-flop after each alternate edge of the second signal, wherein the flip-flop is coupled to the first and second signals.

22. (New) The method of claim 21, wherein the acts of regenerating the clock signal are performed on a line side of a capacitive isolation barrier.

23. (New) The method of claim 21, wherein the act of setting the initial state of the flip-flop comprises setting the initial state of the flip-flop after each rising edge of the second signal.

24. (New) The method of claim 21, wherein the act of setting the initial state of the flip-flop comprises coupling one of the first signal and the second signal to a reset input of the flip-flop.

25. (New) The method of claim 21, wherein the act of shaping comprises:

detecting each alternate edge of the clock signal and shaping the clock signal into a first signal having a single voltage pulse between each alternate edge of the clock signal; and

detecting each alternate edge of the inverted clock signal and shaping the inverted clock signal into a second signal having a single voltage pulse between each alternate edge of the inverted clock signal.

26. (New) The method of claim 21, wherein the act of shaping comprises:

detecting each alternate edge of the clock signal and shaping the clock signal into a first signal having a single voltage pulse between each rising edge of the clock signal; and

detecting each alternate edge of the inverted clock signal and shaping the inverted clock signal into a second signal having a single voltage pulse between each rising edge of the inverted clock signal.

27. (New) The method of claim 21, wherein the act of shaping includes shaping the first and second signals between ground and a reference potential.

28. (New) The method of claim 21, further comprising an act of inputting the first and second signals to a NAND gate.

29. (New) The method of claim 28, wherein the flip-flop is a D-type flip-flop, and wherein the method further comprises an act of inputting an output of the NAND gate to a clock input of the flip-flop.

30. (New) The method of claim 29, wherein the flip-flop comprises a reset input, and wherein the method further comprises an act of inputting the second signal to the reset input.